IN THE SPECIFICATION:

Please amend the specification as follows:

Please substitute the paragraph beginning at page 1, line 5, with the following.

-- The present invention relates to a distortion measurement technique for manufacturing a device such as a semiconductor element, image sensing element (CCD or the like), a liquid crystal display element, a thin-film magnetic head, or the like. --

Please substitute the paragraph beginning at page 1, line 12, with the following.

-- As disclosed in Japanese Patent No. ~~3,959,190~~ 3,259,190, at least five methods are well known as a method of measuring a distortion (distortion component generated when a mask image is transferred onto a wafer) in the projection optical system of an exposure apparatus. --

Please substitute the paragraph beginning at page 1, line 17, with the following.

-- Of these methods, two methods disclosed in Japanese Patent No. ~~3,959,190~~ 3,259,190 and Japanese Publication No. 63-38697 are proposed as a distortion measurement method using overlay of a main scale mark and a vernier scale mark. --

Please substitute the paragraph beginning at page 3, line 5, with the following.

-- (2) Method Disclosed in Japanese Patent No. ~~3,959,190~~ 3,259,190 --

Please substitute the paragraph beginning at page 4, line 6, with the following.

-- However, the conventional distortion measurement methods described above suffer from the following problems. --

Please substitute the paragraph beginning at page 6, line 12, and ending on page 7, line 5, with the following.

-- According to another aspect of the invention, there is provided a method comprising: a first exposure step of exposing each of first shot regions on a substrate to a plurality of first marks aligned at a predetermined interval via a master and a projection optical system; a second exposure step of exposing each of second shot regions on the substrate to a plurality of second marks aligned at the predetermined interval via the master and the projection optical system, the first and second shot regions being so arranged as to make positions of a plurality of transferred first and second marks on the substrate correspond to each other, the plurality of transferred first and second marks being formed due to said first and second exposure ~~step~~ steps, respectively, and the number of the transferred first marks in the first shot region being larger than the number of the transferred second marks in the second shot region; and a calculation step of calculating a distortion amount of the projection optical system based on a positional difference measured for the transferred first and second marks which correspond to each other. --

Please substitute the paragraph beginning at page 10, line 11, and ending on page 11, line 4, with the following.

-- In the first step, the $m_1 \times n_1$ vernier scale marks 1 arranged on the entire reticle surface as shown in Fig. 1A are transferred onto a substrate by one exposure apparatus subjected to distortion inspection (first layer exposure processing). The moving stage of the exposure apparatus is moved by a step in the column direction, and the first layer exposure processing is so done as to successively align the vernier scale marks 1 in a region adjacent in the column direction. This operation is repeated m_2 times. Also, in the row direction, step movement and transfer are so repeated as to successively align the vernier scale marks in a region adjacent in the row direction. This operation is repeated n_2 times in the row direction. That is, step movement by a $p_x \times n_1$ distance in the row direction, or step movement by a $p_y \times m_1$ distance in the column direction, and the first layer exposure processing are repeated $m_2 \times n_2$ times, transferring $m_2 \times n_2$ shots 5 on the substrate, as shown in Fig. 2 (in Fig. 2, $2 \times 2 = 4$ shots). --

Please substitute the paragraph beginning at page 13, line 8, with the following.

-- As shown in Fig. 4B, the distortion amount of the position of each vernier scale mark 8 in a shot 7 transferred onto a substrate is defined as variables dx_1 and dy_1. Fig. 5 shows shots in the first layer aligned such that two shots are adjacent to each other in the vertical and horizontal directions. Each shot is formed by scanning exposure (step and scan type exposure) or by block exposure (step and repeat type exposure) in which a whole shot area is exposed at once. Each shot 9 has errors ex_1, ey_1, and $e\theta_1$ in position and rotation angle that are caused by a stage alignment error. The relative positions between vernier scale marks within each shot are equal. --

Please substitute the paragraph beginning at page 15, line 3, with the following.

-- $\varepsilon_x(n)$, $\varepsilon_y(n)$: quantization errors by rounding. --

Please substitute the paragraph beginning at page 17, line 7, with the following.

-- An exposure control apparatus which executes the distortion measurement method will be explained. Fig. 12 is a block diagram showing the arrangements of an exposure apparatus, an exposure control apparatus, and a mark reading apparatus according to the embodiment. Reference numeral 101 denotes an exposure apparatus which comprises an exposure light source 111, an illumination optical system 112, a light-shielding plate 113, a reticle stage 114, a projection optical system 115, and a wafer stage 116. The reticle stage 114 supports a reticle 121 on which the above-described vernier scale marks and main scale marks are drawn. The wafer stage 116 supports a photosensitive substrate 122. --

Please substitute the paragraph beginning at page 18, line 10, with the following.

-- In step S101, the light-shielding plate 113 is controlled, and exposure processing using, as one shot, the entire surface of the reticle 121 having $m_1 \times n_1$ vernier scale marks is repeated $m_2 \times n_2$ times. In step S102, the light-shielding plate 113 is so controlled as to set $m_2 \times n_2$ main scale marks as one shot. Exposure processing using this shot is repeated $m_1 \times n_1$ times, forming $m_1 \times n_1 \times m_2 \times n_2$ (= N) overlay marks. --

Please substitute the paragraph beginning at page 19, line 19, and ending on page 20, line 16, with the following.

-- Fig. 14 shows the manufacturing flow of a microdevice (e.g., a semiconductor chip such as an IC or LSI, a liquid crystal panel, a CCD, a thin-film magnetic head, a micromachine, or the like). In step 1 (circuit design), a semiconductor device circuit is designed. In step 2 (exposure control data creation), exposure control data (exposure job) of the exposure apparatus is created on the basis of the designed circuit pattern. In step 3 (wafer formation), a wafer is formed using a material such as silicon. In step 4 (wafer process), called a pre-process, an actual circuit is formed on the wafer by lithography using the wafer and the exposure apparatus which has received the prepared exposure control data. At this time, the exposure control data is properly corrected using the correction value 132b, and high-precision exposure processing is executed. Step 5 (assembly), called a post-process, is the step of forming a semiconductor chip by using the wafer formed in step 4, and includes an assembly process (dicing and bonding) and a packaging process (chip encapsulation). In step 6 (inspection), the semiconductor device manufactured in step 5 undergoes inspections such as an operation confirmation test and a durability test. After these steps, the semiconductor device is completed and shipped (step 7). --